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(54) **METHOD AND SYSTEM FOR HETEROGENEOUS SUBSTRATE BONDING OF WAVEGUIDE RECEIVERS**

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This patent is subject to a terminal disclaimer.

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(51) **Int. Cl.**
H01S 5/00 (2006.01)

(52) **U.S. Cl.**
USPC **372/50.21**; 372/43.01; 372/45.01; 372/50.1; 257/731; 257/473; 257/732; 257/E29.002; 257/E33.056; 257/98; 257/99; 257/100; 438/25; 438/26; 438/27

(58) **Field of Classification Search**
USPC 372/43.01–50.23; 257/98–100, 473, 257/731, 732, E29.002, E33.056; 438/25–27
See application file for complete search history.

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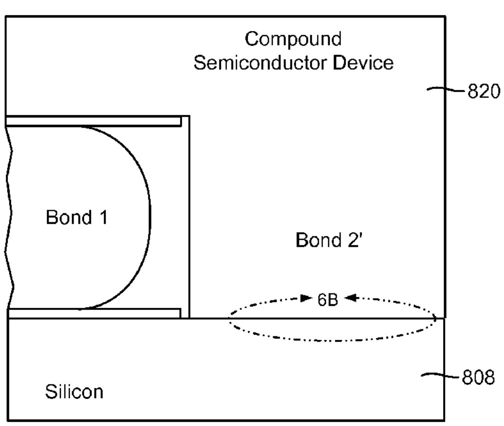
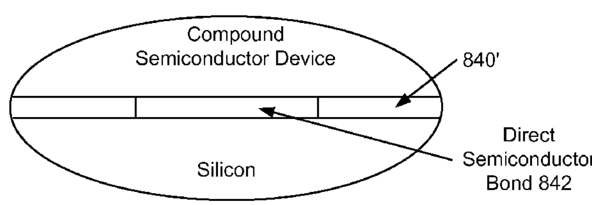
(57) **ABSTRACT**

A composite integrated optical device includes a substrate including a silicon layer and a waveguide disposed in the silicon layer. The composite integrated optical device also includes an optical detector bonded to the silicon layer and a bonding region disposed between the silicon layer and the optical detector. The bonding region includes a metal-assisted bond at a first portion of the bonding region. The metal-assisted bond includes an interface layer positioned between the silicon layer and the optical detector. The bonding region also includes a direct semiconductor-semiconductor bond at a second portion of the bonding region.

12 Claims, 10 Drawing Sheets





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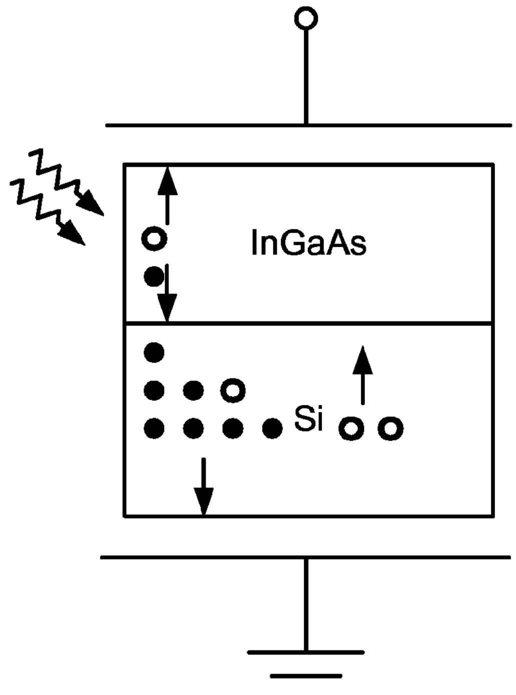

FIG. 1

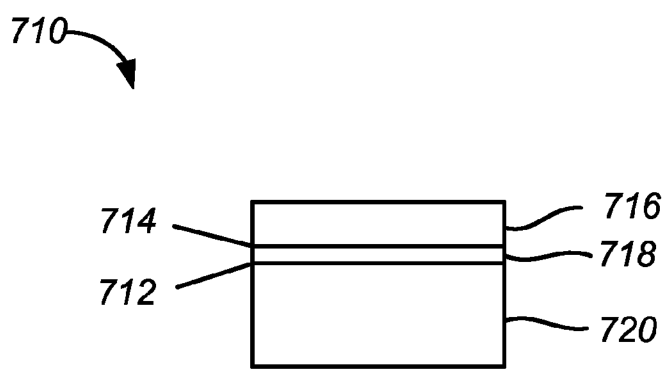

FIG. 2

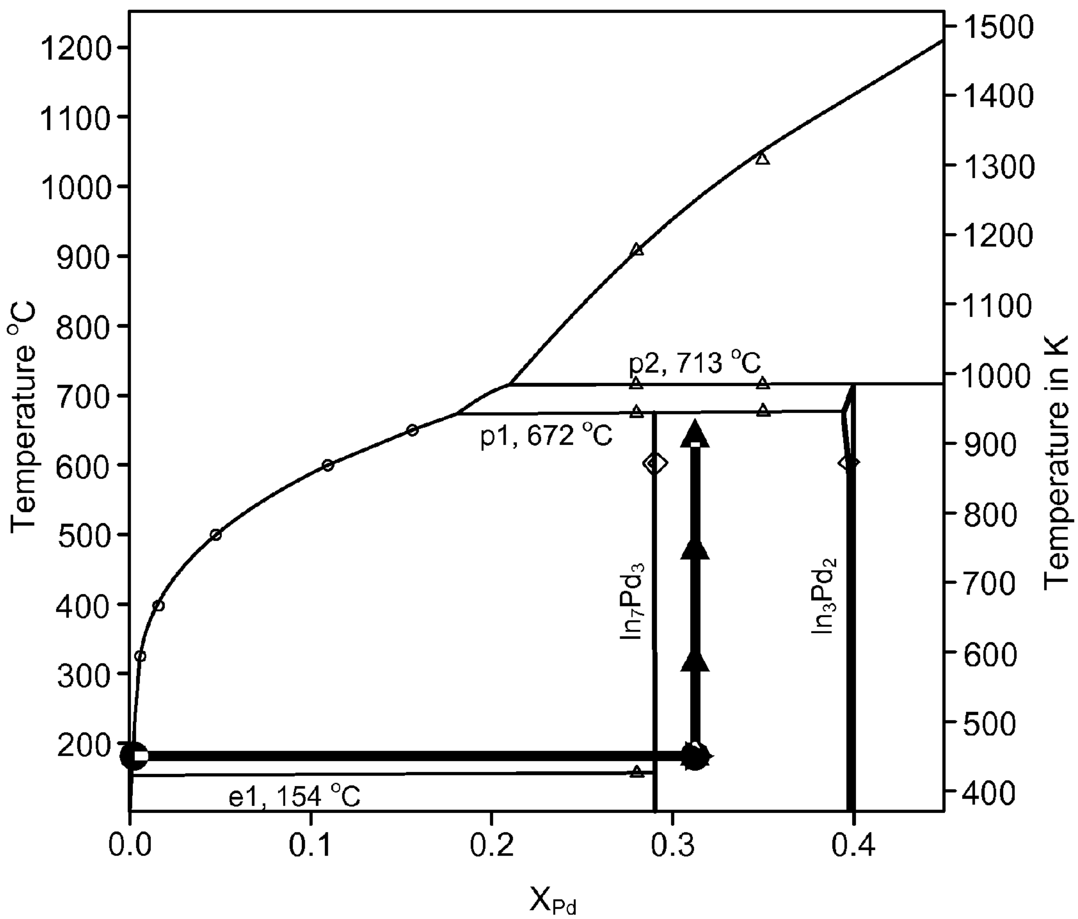
Temperature °C
1200
1100
1000
900
800
700
600
500
400
300
200
Temperature in K
1500
1400
1300
1200
1100
1000
900
800
700
600
500
400
p2, 713 °C
p1, 672 °C
e1, 154 °C
In7Pd3
In3Pd2
0.0
0.1
0.2
0.3
0.4
XPd

FIG. 3

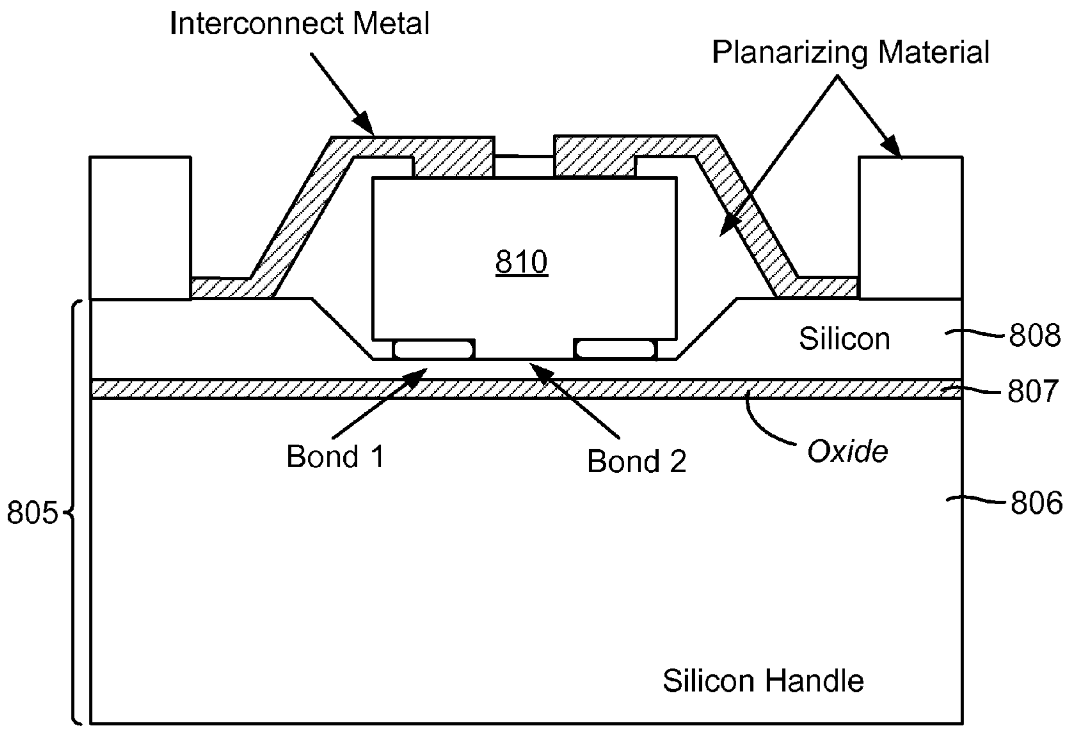
Interconnect Metal
Planarizing Material
810
Silicon
808
807
Bond 1
Bond 2
Oxide
805
806
Silicon Handle

FIG. 4

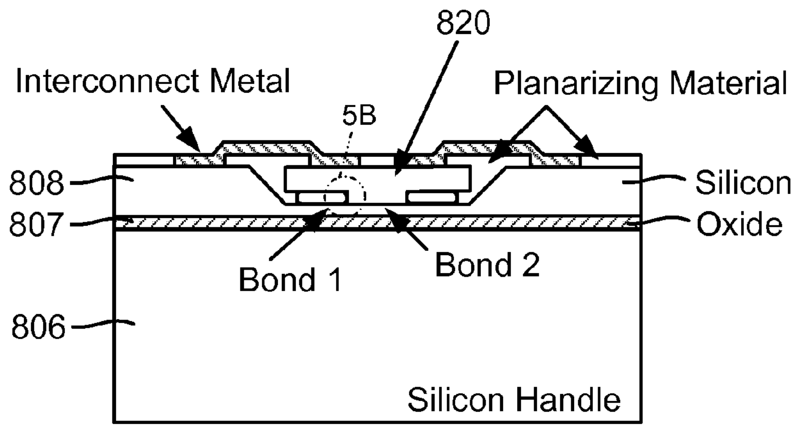

FIG. 5A

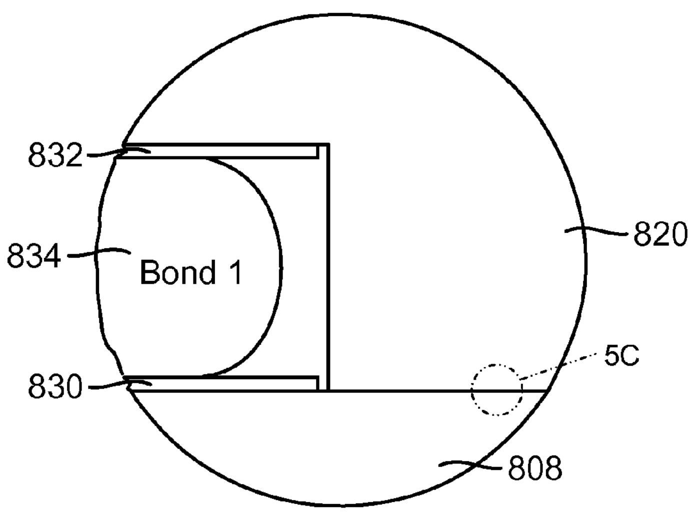

FIG. 5B

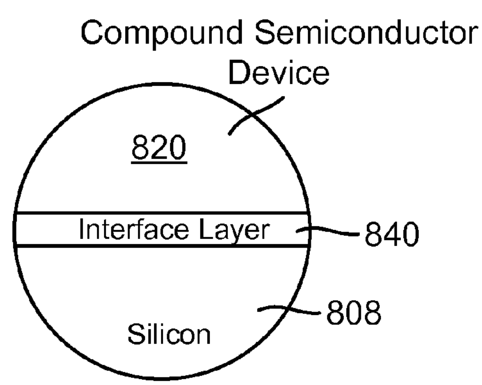

FIG. 5C

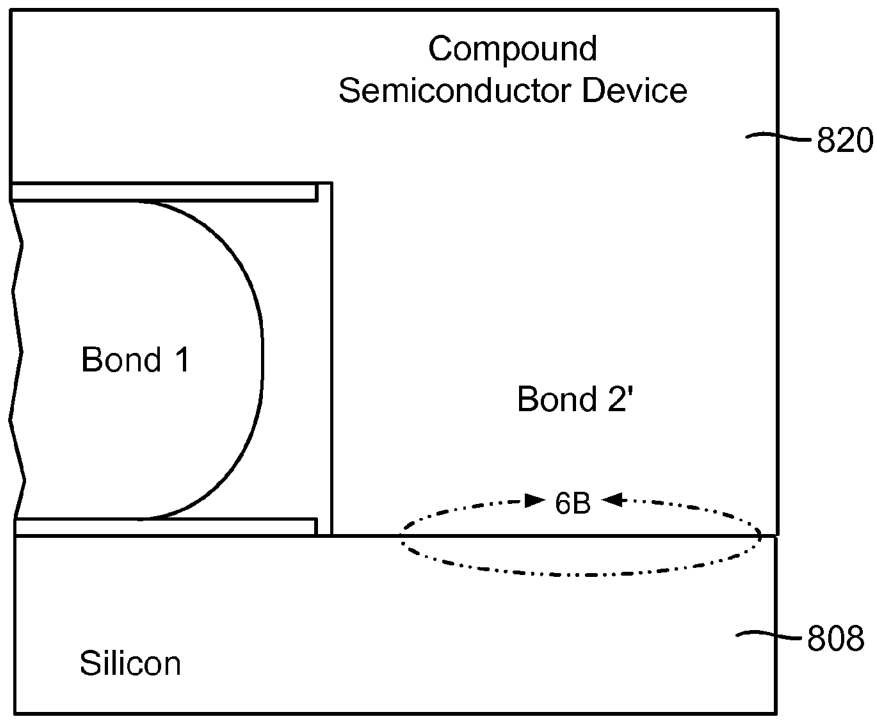
Compound
Semiconductor Device
820
Bond 1
Bond 2'
6B
Silicon
808

FIG. 6A

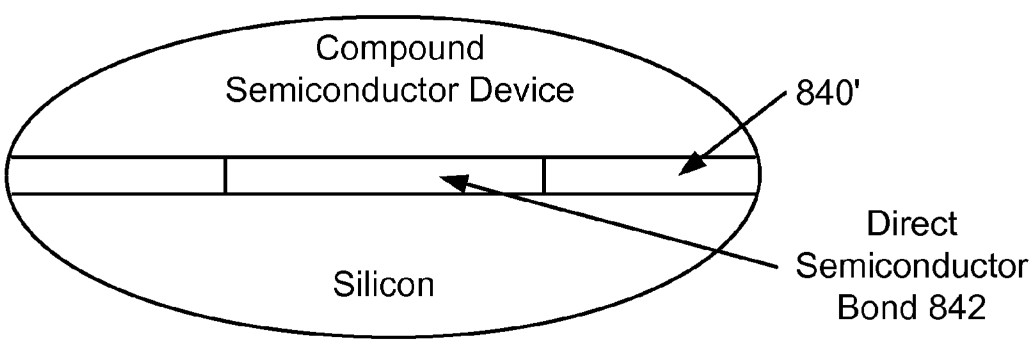
Compound
Semiconductor Device
840'
Direct
Semiconductor
Bond 842
Silicon

FIG. 6B

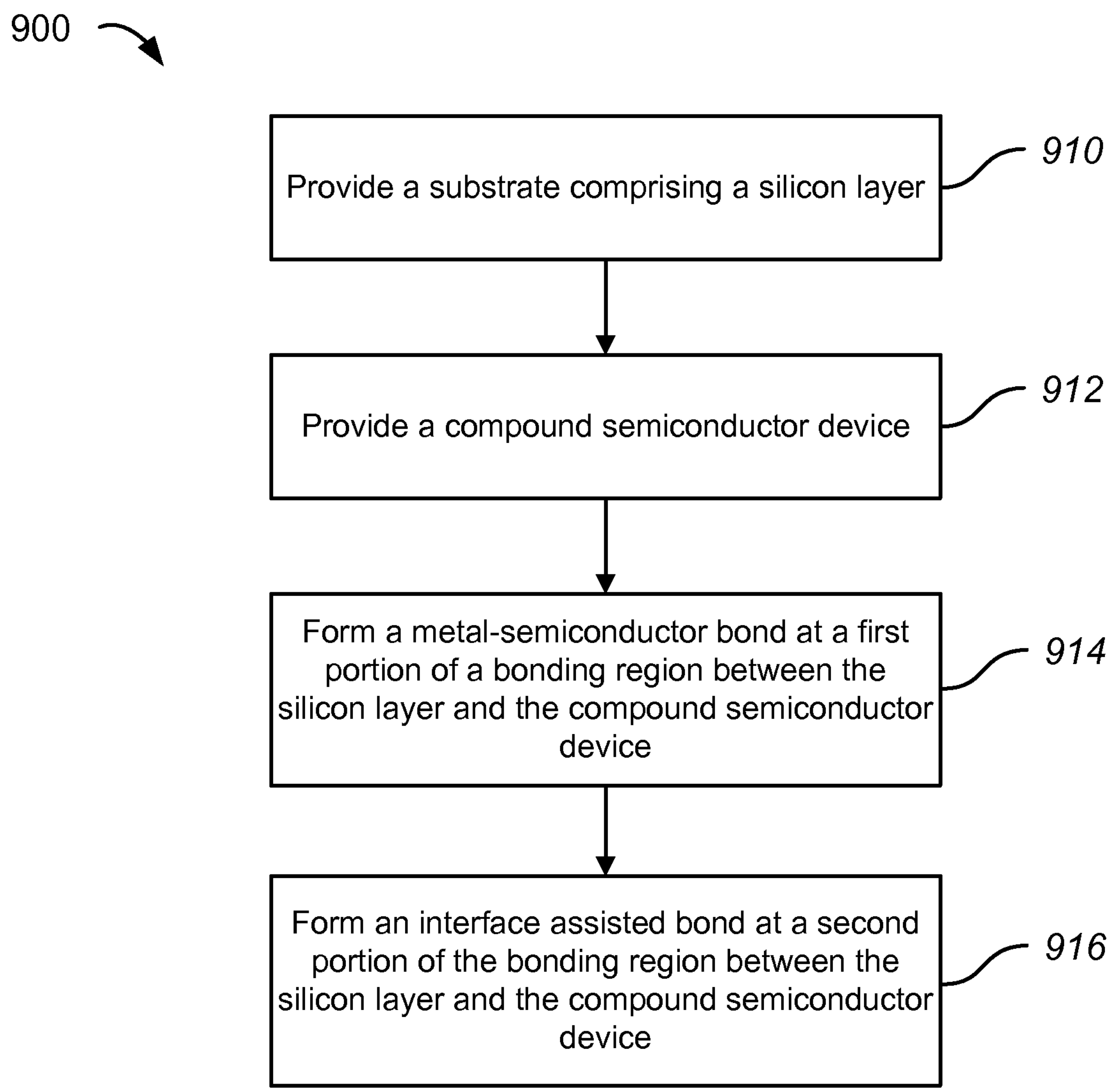
900
Provide a substrate comprising a silicon layer
910
Provide a compound semiconductor device
912
Form a metal-semiconductor bond at a first portion of a bonding region between the silicon layer and the compound semiconductor device
914
Form an interface assisted bond at a second portion of the bonding region between the silicon layer and the compound semiconductor device
916

FIG. 7

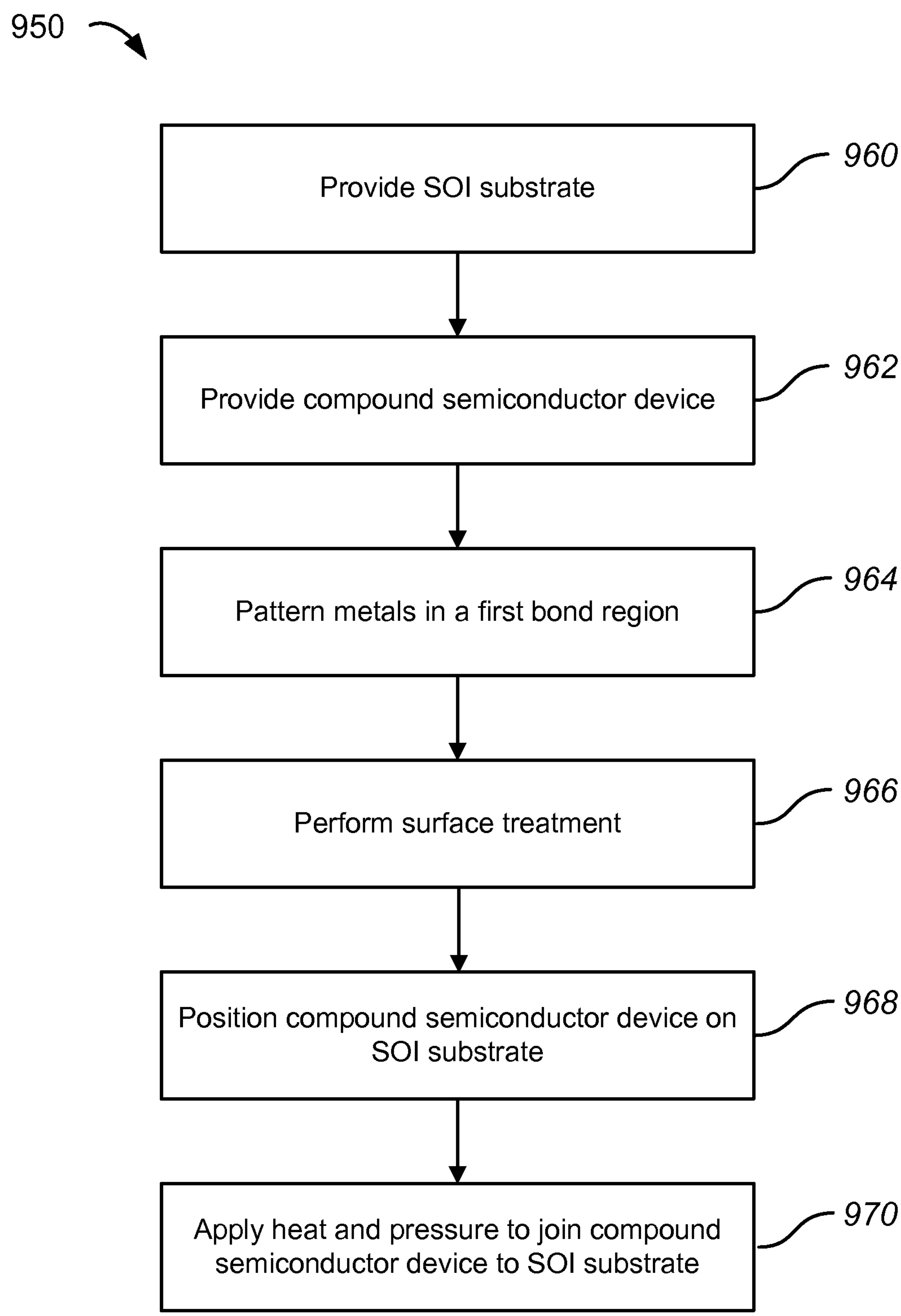
950
Provide SOI substrate
960
Provide compound semiconductor device
962
Pattern metals in a first bond region
964
Perform surface treatment
966
Position compound semiconductor device on SOI substrate
968
Apply heat and pressure to join compound semiconductor device to SOI substrate
970

FIG. 8

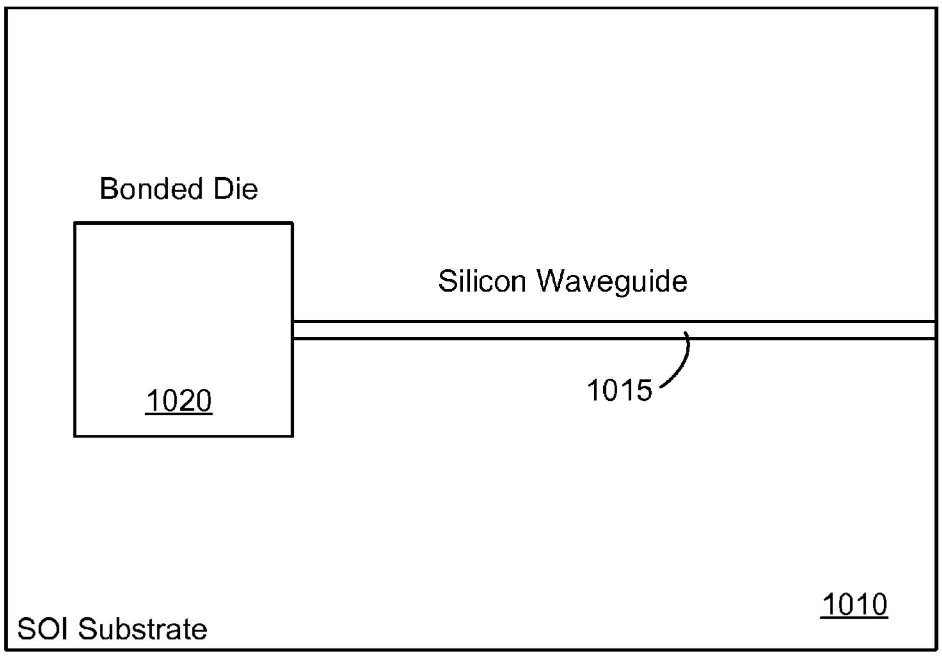
Bonded Die
Silicon Waveguide
1020
1015
SOI Substrate
1010

FIG. 9A

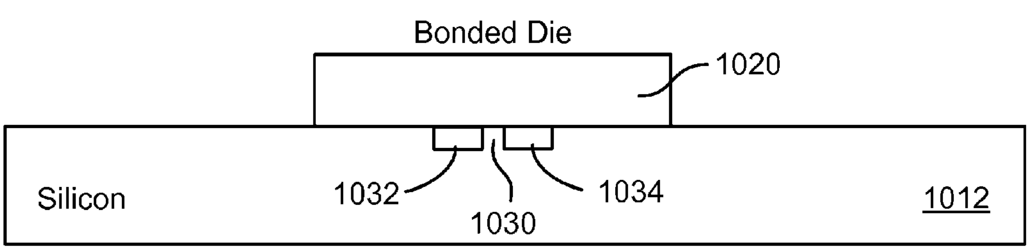
Bonded Die
1020
Silicon
1032
1030
1034
1012

FIG. 9B

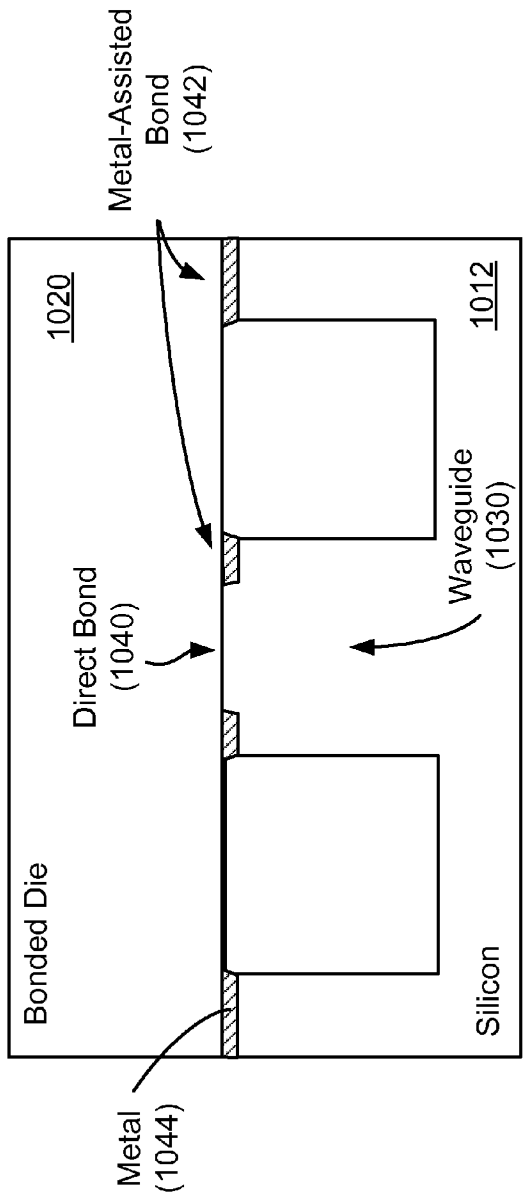
Metal-Assisted Bond (1042)
1020
1012
Bonded Die
Silicon
Direct Bond (1040)
Waveguide (1030)
Metal (1044)

FIG. 10

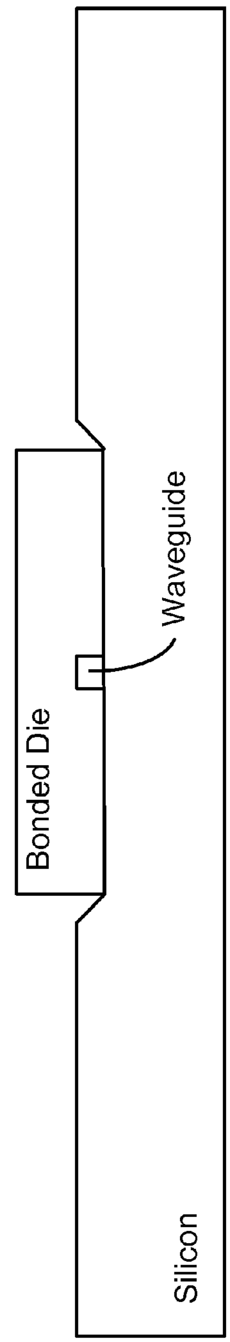
Bonded Die
Waveguide
Silicon

FIG. 11

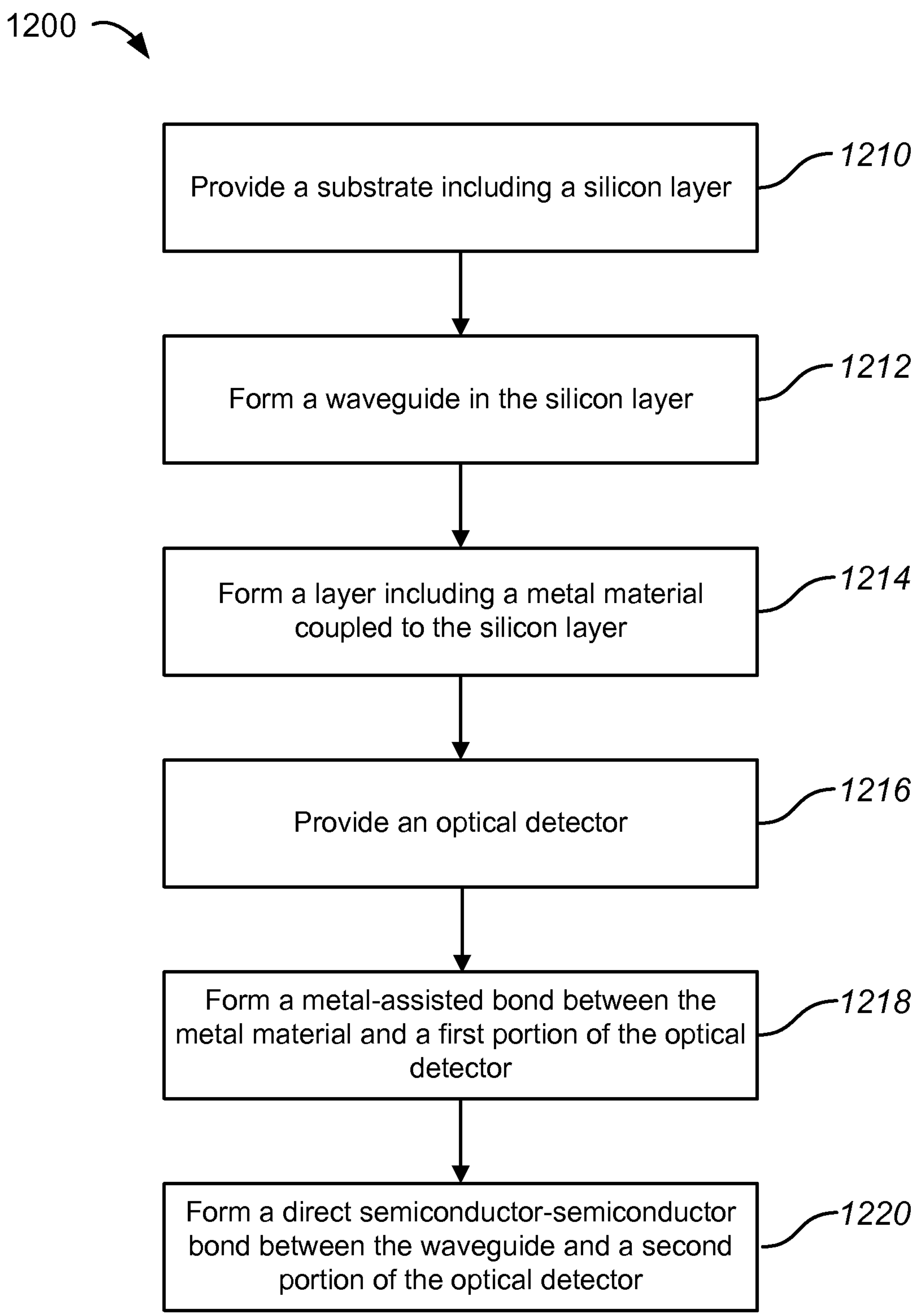
1200
Provide a substrate including a silicon layer
1210
Form a waveguide in the silicon layer
1212
Form a layer including a metal material coupled to the silicon layer
1214
Provide an optical detector
1216
Form a metal-assisted bond between the metal material and a first portion of the optical detector
1218
Form a direct semiconductor-semiconductor bond between the waveguide and a second portion of the optical detector
1220

FIG. 12

METHOD AND SYSTEM FOR HETEROGENEOUS SUBSTRATE BONDING OF WAVEGUIDE RECEIVERS

CROSS-REFERENCES TO RELATED APPLICATIONS

This present application is a continuation-in-part of U.S. patent application Ser. No. 12/902,621, filed on Oct. 12, 2010, which claims priority to U.S. Provisional Patent Application No. 61/251,132, filed on Oct. 13, 2009, the disclosures of which are hereby incorporated by reference in their entirety for all purposes. U.S. patent application Ser. No. 12/902,621 was filed concurrently with 12/903,025, the disclosure of which is hereby incorporated by reference in its entirety for all purposes.

BACKGROUND OF THE INVENTION

Silicon integrated circuits ("ICs") have dominated the development of electronics and many technologies based upon silicon processing have been developed over the years. Their continued refinement led to nanoscale feature sizes that can be critical for making complementary metal oxide semiconductor CMOS circuits. On the other hand, silicon is not a direct bandgap materials. Although direct bandgap materials, including III-V compound semiconductor materials, such as indium phosphide, have been developed, there is a need in the art for improved methods and systems related to photonic ICs utilizing silicon substrates.

SUMMARY OF THE INVENTION

According to an embodiment of the present invention, techniques related to semiconductor fabrication processes are provided. Merely by way of example, embodiments of the present invention have been applied to methods and systems for bonding heterogeneous substrates for use in photonic integration applications. More particularly, an embodiment of the present invention utilizes a hybrid bonding structure including a metal/semiconductor bond and a semiconductor/semiconductor bond in order to achieve low optical loss and high electrical conductivity. The semiconductor/semiconductor bond may be an interface assisted bond. However, the scope of the present invention is broader than this application and includes other substrate bonding techniques. Throughout this specification, the term "composite bonding" can be used interchangeably with the term "hybrid bonding" and the term "composite device" can be used interchangeably with the term "hybrid device."

According to an embodiment of the present invention, a composite integrated optical device is provided. The composite integrated optical device includes a substrate including a silicon layer and a waveguide disposed in the silicon layer. The composite integrated optical device also includes an optical detector bonded to the silicon layer and a bonding region disposed between the silicon layer and the optical detector. The bonding region includes a metal-assisted bond at a first portion of the bonding region. The metal-assisted bond includes an interface layer positioned between the silicon layer and the optical detector. The bonding region also includes a direct semiconductor-semiconductor bond at a second portion of the bonding region.

According to another embodiment of the present invention, a method of fabricating a composite integrated optical device is provided. The method includes providing a substrate comprising a silicon layer and forming a waveguide in the silicon

layer. The method also includes forming a layer comprising a metal material coupled to the silicon layer and providing an optical detector. The method further includes forming a metal-assisted bond between the metal material and a first portion of the optical detector and forming a direct semiconductor-semiconductor bond between the waveguide and a second portion of the optical detector.

Numerous benefits are achieved by way of the present invention over conventional techniques. For example, embodiments of the present invention provide methods and systems suitable for providing a bond with good mechanical strength, good electrical conductivity, sufficient compliance to allow the composite or hybrid bonding of semiconductor materials with different coefficients of thermal expansion with good reliability, and which also has good optical transparency. This combination of benefits allows both electrical and optical functionality across the bonded interface between two or more distinct semiconductor materials. These and other embodiments of the invention along with many of its advantages and features are described in more detail in conjunction with the text below and attached figures.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates an example of a photodiode with a low stress bond between a III-V substrate and a silicon substrate;

FIG. **2** illustrates a bonded structure according to an embodiment of the present invention;

FIG. **3** illustrates a phase diagram showing alloy stability according to an embodiment of the present invention;

FIG. **4** is a simplified schematic diagram of a compound semiconductor structure bonded to a silicon substrate according to an embodiment of the present invention;

FIGS. **5**A-**5**C are simplified schematic diagrams illustrating bond interfaces according to an embodiment of the present invention;

FIGS. **6**A-**6**B are simplified schematic diagrams illustrating bond interfaces according to another embodiment of the present invention;

FIG. **7** is a simplified flowchart illustrating a method of fabricating a hybrid semiconductor structure according to an embodiment of the present invention;

FIG. **8** is a simplified flowchart illustrating a method of fabricating a hybrid semiconductor structure according to another embodiment of the present invention;

FIG. **9**A is a simplified plan view illustrating a composite-bonded die joined to a silicon photonic substrate according to an embodiment of the present invention;

FIG. **9**B is a simplified side view of the composite-bonded die and silicon photonic substrate illustrated in FIG. **7**A;

FIG. **10** is a magnified view of the interface between the composite-bonded die and silicon photonic substrate illustrated in FIG. **7**B;

FIG. **11** is a simplified side view illustrating a composite-bonded die joined to a silicon photonic substrate including direct coupling according to an embodiment of the present invention; and

FIG. **12** is a simplified flowchart illustrating a method of fabricating a composite integrated optical device according to an embodiment of the present invention.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

Embodiments of the present invention relate to an apparatus and method that preferably uses a bonding stress for wafer bonding and utilizes an intermediate layer to facilitate the transition from silicon and the like to another material for optical coupling as well as electron transport. Embodiments of the present invention preferably incorporate low stress, low temperature wafer bonding known in the industry and preferably comprise a thin film intermediate layer for optical coupling as well electron transport.

FIG. **1** illustrates an example of a photodiode with a low stress bond between a III-V substrate and a silicon substrate. FIG. **2** illustrates a bonded structure according to an embodiment of the present invention. As illustrated in FIG. **2**, two interfaces **712** and **714** are provided. First interface **712** is positioned between a silicon substrate **720** and an intermediate layer **718**. Second interface **714** is located between intermediate layer **718** and a second semiconductor layer **716**. Embodiments of the present invention are preferably used in the bonding process to facilitate integration of heterogeneous materials. Embodiments that facilitate integration preferably share the stress due to lattice mismatch between the silicon crystal and the second semiconductor that can form at these two interfaces and can be greatly reduced because of the reduced need for crystalline in the intermediate layer. The intermediate layer can be an alloy whose composition can be graded across the layer to facilitate the bonding at both interfaces **712** and **714**.

Intermediate layer **718** is preferably thin, ranging from between approximately 4-5 monolayers to more than approximately 60-70 monolayers, substantially allowing the optical and thermal conduction properties to be virtually unaffected while the electron transport can preferably be achieved via actual carrier transport across the layer. In some embodiments of the present invention, intermediate layer **718** forms thermal and electric contacts at both the first interface and second interface. Embodiments of the present invention can be used in the fabrication of a plurality of high performance optoelectronic components, including but not limited to modulators, lasers, detectors, amplifiers, couplers, wavelength tunable optical components and/or circuits, combinations thereof, or the like. Embodiments as described herein are applicable to a variety of material systems including silicon as illustrated by silicon substrate **720** and/or the like and second semiconductor materials **716**, which can be a compound semiconductor material. Utilizing embodiments of the present invention, heterogeneous materials (e.g., compound semiconductors and silicon substrates can be integrated on a common substrate.

The term "bandgap" as used throughout this application includes but is not limited to the energy difference between the top of the valence band and the bottom of the conduction band. The term "optical coupling" as used throughout this application includes but is not limited to placing two or more electromagnetic elements including optical waveguides close together so that the evanescent field generated by one element does not decay much before it reaches the other element. The term "electron transport" as used throughout this application includes but is not limited to an electron transport chain coupling a chemical reaction between an electron donor and an electron acceptor to the transfer of H^+ ions across a membrane, through a set of mediating chemical or biochemical reactions. In the case of p-n junctions or interfaces between p-type material, especially in the case of direct semiconductor bonding, holes, as opposed to electrons, may be transported across the interface. The term "complementary metal oxide semiconductor" as used throughout this application includes but is not limited to technologies for making integrated circuits, microprocessors, microcontrollers, static RAM, digital logic circuits, analog circuits, and highly integrated transceivers.

Embodiments of the present invention optionally utilize several features of intermediate layer **718** as illustrated in FIG. **2**. According to an embodiment, the thickness of the intermediate layer **718** is very thin, ranging from a few monolayers (i.e., around 10 Å in thickness) to tens of monolayers. In an embodiment, the intermediate layer is deposited using a deposition technique that provides for uniform coverage at small thicknesses. Exemplary deposition techniques include PVD, ALD, sputtering, e-beam deposition, or the like. Intermediate layer **718** is preferably deposited at relatively low temperatures ranging from temperatures less than 200° C. At these low temperatures, there preferably exist small differences of thermal expansion (i.e., differences in the coefficient of thermal expansion (CTE)) between first interface **712** and second interface **714**. Intermediate layer **718** preferably forms thermal contacts at the interfaces and is preferably thermally conductive. Intermediate layer **718** preferably forms good electrical contacts at both interfaces and is preferably electrically conductive. It is not necessary to be crystalline in nature so that the lattice matching at both interfaces is not an issue. In some embodiments, intermediate layer **718** is an alloy material for which the composition varies across the layer.

It should be noted that the alloy may or may not vary in composition since the composition can depend, for example, on the composition of the initial layer stack and the alloying process. Preferably, the wafer bonding process and the thermal profile associated with the wafer bonding process will result in the metal becoming a uniform alloy. Thus, compositional grading is not required for stress accommodation. In other embodiments, a compositional gradient could be present as appropriate to the particular application.

Embodiments of the present invention are applicable to an apparatus that includes a semiconductor layer that is provided over an intermediate layer that is provided over a silicon substrate layer. The intermediate layer has a lower thermal conductivity than the semiconductor layer. The apparatus also includes a plurality of interfaces that are provided between the semiconductor layer and the underlying layer(s), thereby preventing crystalline lattice mismatch.

Embodiments of the present invention also include a bonding method including forming first and second bonding surfaces on first and second materials, respectively, at least one of the bonding surfaces including an intermediate layer. The method also includes enhancing activation of at least one of said first and second bonding surfaces, terminating at least one of said first and second bonding surfaces with species allowing formation of chemical and electrical bonds, and annealing said first and second materials at a temperature.

FIG. **3** illustrates a phase diagram showing alloy stability according to an embodiment of the present invention. As illustrated in FIG. **3**, the stability of the alloy makes such an alloy suitable for use as an intermediate layer such as intermediate layer **718**. In some embodiments, the alloy (e.g., In_xPd_y) has a small thickness to accommodate stress at the semiconductor-semiconductor interface.

While the embodiments of the invention described herein are directed to wafers used in the semiconductor industry, the invention is also applicable to thermoelectric (TE) cooling technology as well as virtually any application including optical coupling and electron transport.

Merely by way of example, an intermediate layer suitable for use according to embodiments of the present invention is In_xPd_y, for example, $In_{0.7}Pd_{0.3}$, which is an alloy that is stable up to very high temperatures as illustrated in FIG. **3**. This alloy forms an ohmic contact at interfaces with both silicon and/or III-V materials for which the doping types at either side can be either p-type or n-type. Thus, embodiments of the present invention provide an intermediate layer that provides both ohmic contact between materials on both sides of the intermediate layer, adhesion, optical quality including transparency (i.e., low optical loss), stress accommodation, and other benefits. Other suitable alloys include germanium palladium, gold/germanium, Au/Sn, Al/Mg, Au/Si, palladium, indium/tin/silver alloys, metal alloys containing Bi, Sn, Zn, Pb, or In, combinations thereof, or the like. The optimal alloy will generally have eutectic or peritectic points, and will allow a bonding process temperature in the 350° C. to 500° C. range.

It should be noted that although in some embodiments, an ohmic contact is formed, it may be useful to form other types of contacts, particularly in the regions where direct semiconductor bonding is used instead of metal-assisted bonding. Examples of contacts other than ohmic contacts include tunnel junctions, p-n junctions, heterojunctions, or the like. For instance, for the implementations including metal-assisted bonding, Schottky contacts will be useful in some applications.

FIG. **4** is a simplified schematic diagram of a compound semiconductor structure bonded to a silicon substrate according to an embodiment of the present invention. Referring to FIG. **4**, a composite metal/semiconductor bond is illustrated in relation to bonding of a compound semiconductor device **810** to a silicon-based substrate **805**. In the embodiment illustrated in FIG. **4**, the silicon-based substrate **805** is a silicon-on-insulator (SOI) substrate although this is not required by embodiments of the present invention. The SOI substrate includes a silicon handle layer **806**, a silicon oxide layer **807**, and a silicon layer **808**, which may be single crystal silicon. Planarizing material is used in the embodiment illustrated in FIG. **4** as well as an interconnect metal that provides for electrical conductivity between portions of the compound semiconductor device **810** and the silicon layer **808** of the SOI substrate. In the embodiment illustrated in FIG. **4**, the compound semiconductor device **810** extends to a height above the top surface of the silicon layer **808**.

As illustrated in FIG. **4**, several bonds are formed between silicon layer **808** and the compound semiconductor device **810**. Bond **1** is a metal/metal bond. Associated with Bond **1**, pads (not shown in FIG. **4** but illustrated in following figures) are defined on both the SOI substrate (e.g., silicon layer **808**) and the compound semiconductor device **810**. These pads can include an adhesion metal such as Ti or Cr and a barrier metal such as Pt or Ni. The metal used for the bonding process will typically be a eutectic solder with a eutectic point in the 350° C.-500° C. range. An example of such a eutectic solder is AuGe.

Bond **2** as illustrated in FIG. **4** can be either a direct semiconductor/semiconductor bond or a metal-assisted semiconductor/semiconductor bond. For the metal-assisted semiconductor/semiconductor bond, a thin metal layer (e.g., ranging from one to a few monolayers to a few tens of monolayers) is deposited to improve the robustness of the interface and to better accommodate the CTE differences between silicon and the compound semiconductor device. In an embodiment, the thin metal layer is less than 50 Å in thickness. The very thin interfacial metal will still allow light to pass through without significant attenuation. The direct semiconductor/semiconductor bond can be formed using techniques including either chemical activation or plasma activation of the surfaces and joining the materials together with pressure and low temperature in order to bond the two surfaces together. Direct semiconductor bonding is useful in devices employing evanescent coupling in a waveguide structure as it will have lower optical attenuation than metal-assisted semiconductor bonding.

FIGS. **5**A-**5**C are simplified schematic diagrams illustrating bond interfaces according to an embodiment of the present invention. As illustrated in FIG. **5**A, the compound semiconductor device **820** has been thinned so that the top surface of the compound semiconductor device **820** is coplanar with the top surface of silicon layer **808**. A planarizing material has been used to provide a planar surface extending above the top surface of silicon layer **808**. Portions of the planarizing material have been removed (e.g., using a masking and etching process) and interconnect metals have been used to provide for electrical connectivity between portions of the silicon layer **808** and portions of the compound semiconductor device **820**.

FIG. **5**B illustrates additional details related to Bond **1** including pads **830** and **832** that provide for adhesion between the silicon layer **808**, the bonding metal **834** and the compound semiconductor device **820**. As discussed in relation to FIG. **4**, pads **830** and **832** can include an adhesion metal such as Ti or Cr and a barrier metal such as Pt. The bonding metal **834** can be a eutectic solder such as AuGe. Other pad materials include Ni, W, refractory metals used as barrier layers in silicon-based devices, or the like, and other bonding metals include AuSn, InPd, InSn, InSnAg alloys, combinations thereof, or the like. These materials are listed merely by way of example and other materials that provide for adhesion between surfaces and/or barrier functionality are also included within the scope of the present invention.

FIG. **5**C illustrates the use of an interface layer **840** between the compound semiconductor device **820** and the silicon layer **808**. As discussed previously, the metal-assisted semiconductor/semiconductor bond illustrated in FIG. **5**C includes a thin metal layer that provides beneficial functions including improving the robustness of the interface and accommodating CTE differences between the materials bonded to either side of this interface layer. Interface layers can include suitable materials including materials that provide peritectic properties including metals such as InPd, other metal alloys, combinations thereof, or the like. Gettering materials such as Ti or Cr can also be integrated with the interface layer to getter surface oxides and improve bond properties. For thin layers of interfacial metals, light will be able to pass without significant attenuation. The low optical loss provided by embodiments of the present invention include absorption coefficients that can be computed using waveguide models and the measured absorption properties of the interface layer. The use of an interface layer **840** will also provide an ohmic contact between the silicon layer **808** and the compound semiconductor device **820**. Thus, embodiments of the present invention provide an interface that is electrically conductive without significant optical absorption.

Although FIGS. **5**A-**5**C illustrate bonding of a compound semiconductor device to an SOI substrate, embodiments of the present invention are not limited to the bonding of a device to a substrate. Other embodiments of the present invention are applicable to substrate to substrate bonding, also referred to as wafer bonding. Thus, the compound semiconductor device illustrated in the figures can be replaced with a compound semiconductor substrate in the processes and structures described herein. One of ordinary skill in the art would recognize many variations, modifications, and alternatives.

As illustrated in FIG. **5**C, an interface layer **840** such as a thin layer (e.g., less than 100 Å) of a metal alloy such as In_xPd_y, can be used to accommodate some of the CTE mismatch between the two semiconductor materials. In other embodiments, the interface layer is not present and a direct semiconductor/semiconductor bond is formed for Bond **2**. Embodiments of the present invention utilize both a metal/metal bond illustrated by Bond **1** and a direct semiconductor/semiconductor bond or an interface assisted semiconductor/semiconductor bond illustrated by Bond **2**. Such a hybrid bonding approach utilizes the benefits provided by both types of bonds to reduce or overcome the disadvantages of low temperature semiconductor/semiconductor bonding including the weak interface as well as the disadvantages of metal/metal bonding including high optical loss in the vicinity of the metal/metal bond. Thus, embodiments of the present invention provide for high strength bonds and electrical conductivity (Bond **1**) while enabling low optical loss and electrical conductivity in regions of the structure suitable for light propagation (Bond **2**). Throughout this specification, the term "composite integration/bonding" can be used interchangeably with the term "hybrid integration/bonding."

FIGS. **6**A-**6**B are simplified schematic diagrams illustrating bond interfaces according to another embodiment of the present invention. In the case where light propagates parallel to the interface formed at Bond **2** and evanescent coupling is used between the silicon layer **808** and the compound semiconductor device **820**, a combination of direct semiconductor-semiconductor bonding and metal-assisted semiconductor-semiconductor bonding may be employed to form Bond **2**. This can be achieved by selective patterning of the thin interfacial metal. Referring to FIG. **6**A, Bond **2'** between the silicon layer **808** and the compound semiconductor device **810** is illustrated. Bond **2'** includes not only an interface layer **840'** similar to layer **840** in FIG. **5**C, but a direct semiconductor-semiconductor bond **842**. In the embodiment illustrated in FIG. **6**B, the interface layer **840'** is patterned to provide regions that are free of the interface layer, which may be a metal layer. As an example, in a light emitting device, the direct semiconductor-semiconductor bond could be positioned adjacent the light emission region to prevent absorption of light by the interface layer. The combination of an interface layer with a direct semiconductor-semiconductor bond thus provides benefits associated with each of the bonding techniques in a hybrid manner.

The bonding processes described herein can be performed in the temperature range from about 350° C. to about 500° C. In a particular embodiment, the temperature associated with the bonding process is in the temperature range of 400° C.-450° C. These temperatures are below the temperature at which CMOS circuits, which may be previously fabricated on the SOI substrate, would be damaged. This enables the integration of complex electrical functions while still providing a robust bond between the dissimilar materials discussed herein.

FIG. **7** is a simplified flowchart illustrating a method of fabricating a hybrid semiconductor structure according to an embodiment of the present invention. The method **900** includes providing a substrate comprising a silicon layer (**910**), providing a compound semiconductor device (e.g., an InP semiconductor laser) (**912**), and forming a bonding region disposed between the silicon layer and the compound semiconductor device. Forming the bonding region includes forming a metal-semiconductor bond at a first portion of the bonding region (**914**). The metal-semiconductor bond includes a first pad bonded to the silicon layer, a bonding metal bonded to the first pad, and a second pad bonded to the bonding metal and the compound semiconductor device. Forming the bonding region also includes forming an interface assisted bond at a second portion of the bonding region (**916**). The interface assisted bond includes an interface layer (e.g., In_xPd_y) positioned between the silicon layer and the compound semiconductor device. The interface assisted bond provides an ohmic contact between the silicon layer and the compound semiconductor device. In an embodiment, the interface layer has a thickness less than 50 Å.

According to an embodiment, the substrate includes an SOI wafer including a silicon substrate, an oxide layer disposed on the silicon substrate, and the silicon layer is disposed on the oxide layer. In embodiments utilizing a laser or other light generator, the second portion of the bonding region can be substantially free from the interface layer at a position adjacent an active region of the laser or optical generator in order to reduce optical losses. The bonding processes can be performed using low temperature bonding processes, for example, at a temperature ranging from about 350° C. to about 500° C., more particularly, from about 400° C. to about 450° C.

It should be appreciated that the specific steps illustrated in FIG. **7** provide a particular method of fabricating a hybrid semiconductor structure according to an embodiment of the present invention. Other sequences of steps may also be performed according to alternative embodiments. For example, alternative embodiments of the present invention may perform the steps outlined above in a different order. Moreover, the individual steps illustrated in FIG. **7** may include multiple sub-steps that may be performed in various sequences as appropriate to the individual step. Furthermore, additional steps may be added or removed depending on the particular applications. One of ordinary skill in the art would recognize many variations, modifications, and alternatives.

FIG. **8** is a simplified flowchart illustrating a method of fabricating a hybrid semiconductor structure according to another embodiment of the present invention. The method **950** includes providing an SOI substrate (**960**) and providing a compound semiconductor device (**962**), which can also be referred to as a compound semiconductor die. In an embodiment of the present invention, the SOI substrate includes one or more optical components such as waveguides, optical isolators, reflective structures, or the like and the compound semiconductor device is an InP gain medium.

The method also includes patterning metals in a first bond region (**964**). The metals can be deposited or formed in a variety of manners. The first bond region can be used for metal-metal bonding and/or for metal-assisted semiconductor-semiconductor bond on one or both materials. After the metals are patterned, a surface treatment is performed (**966**), for example, a chemical treatment of the surface(s), a plasma activation for a semiconductor-semiconductor bond without metal assist, or the like. The surface treatment can be performed in a controlled atmosphere such as an inert environment, a reduced pressure atmosphere such as a vacuum, or the like. The method further includes positioning the compound semiconductor device on the SOI substrate, such as a receptor site (**968**) and applying heat and pressure to join the compound semiconductor device to the SOI substrate (**970**). In an embodiment, the joining step simultaneously effects both metal-based and semiconductor-based bonds.

FIG. **9**A is a simplified plan view illustrating a composite-bonded die joined to a silicon photonic substrate according to an embodiment of the present invention. As illustrated in FIG. **9**A, a die **1020**, which can include a III-V material, a magnetic material, or the like, is bonded to a silicon photonic substrate **1010**, illustrated as an SOI substrate. In a particular embodiment, the bonded die includes an avalanche photodiode (APD) waveguide receiver (i.e., an optical detector) suitable for use in an optical communications system. A silicon waveguide **1015** is formed in the silicon photonic substrate **1010** as discussed throughout the present specification. As an example, the SOI substrate can include a silicon substrate, an oxide layer, and a silicon layer, which can be a single crystal silicon layer. In some embodiments, the silicon waveguide **1015** is formed in the silicon layer (e.g., a single crystal silicon layer) of the silicon photonic substrate **1010**. As described more fully below, light propagating in the silicon waveguide **1015** is coupled into the bonded die, where the light is absorbed as part of a detection process in some embodiments. Thus, embodiments of the present invention provide a waveguide photodiode integrated onto a silicon photonic IC substrate.

FIG. **9**A is a simplified plan view illustrating a composite-bonded die joined to a silicon photonic substrate according to an embodiment of the present invention. As illustrated in FIG. **9**A, a die **1020**, which can include a III-V material, a magnetic material, or the like, is bonded to a silicon photonic substrate **1010**, illustrated as an SOI substrate. In a particular embodiment, the bonded die includes an avalanche photodiode (APD) waveguide receiver suitable for use in an optical communications system. A silicon waveguide **1015** is formed in the silicon photonic substrate **1010** as discussed throughout the present specification. As an example, the SOI substrate can include a silicon substrate, an oxide layer, and a silicon layer, which can be a single crystal silicon layer. In some embodiments, the silicon waveguide **1015** is formed in the silicon layer (e.g., a single crystal silicon layer) of the silicon photonic substrate **1010**. As described more fully below, light propagating in the silicon waveguide **1015** is coupled into the bonded die, where the light is absorbed as part of a detection process in some embodiments. Thus, embodiments of the present invention provide a waveguide photodiode integrated onto a silicon photonic IC substrate.

FIG. **9**B is a simplified side view of the composite-bonded die and silicon photonic substrate illustrated in FIG. **9**A. In the waveguide receiver illustrated in FIG. **9**B, evanescent coupling is used to couple light into the absorption region of the bonded die. Referring to FIG. **9**B, a light propagation region **1030** characterized by a first index of refraction (also referred to as a waveguide) is positioned between cladding regions **1032** and **1034** characterized by a second index of refraction less than the first index of refraction. The cladding regions can be formed by etching trenches and then filling the trenches with a planarizing material. In some embodiments, the cladding regions include air or other suitable gases. In other embodiments, an oxide or other suitable passivating material is deposited and planarized to form the cladding regions. Thus, one or more waveguides can be formed in silicon layer **1012**. Light produced or received at another region of the device can thus propagate with acceptable loss to the bonded die.

FIG. **10** is a magnified view of the interface between the composite-bonded die and silicon photonic substrate illustrated in FIG. **9**B. The expanded view of the interface between the bonded die and the silicon shows a metal layer that has been patterned using a predetermine pattern to allow for a combination of direct semiconductor bonding and metal-assisted bonding.

Bond **1040** is a direct semiconductor/semiconductor bond between the material of the die (e.g., a semiconductor material) and the silicon material of silicon layer **1012**. The direct semiconductor/semiconductor bond can be formed using techniques including either chemical activation or plasma activation of the surfaces and joining the materials together with pressure and low temperature in order to bond the two surfaces together. Direct semiconductor bonding is useful in devices employing evanescent coupling in a waveguide structure as it will have lower optical attenuation than metal-assisted semiconductor bonding. As illustrated in FIG. **10**, the direct bond is formed at a location at which the mode propagating in the waveguide is a maximum, thereby providing a low loss waveguide suitable for a variety of applications. Evanescent coupling enables the light propagating in the waveguide **1030** to couple through the direct bond region into the bonded die, enabling, for example, detector applications.

Bond **1042** is a metal-assisted semiconductor/semiconductor bond. For the metal-assisted semiconductor/semiconductor bond, a thin metal layer **1044** (e.g., ranging from one to a few monolayers to a few tens of monolayers) is deposited and patterned to improve the robustness of the interface and to better accommodate the CTE differences between silicon of silicon layer **1012** and the compound semiconductor material of the die. In an embodiment, the thin metal layer (e.g., an InPd-based metal layer) is less than 50 Å in thickness. As discussed above, the very thin interfacial metal will allow light to propagate through the metal layer (i.e., in a vertical direction in FIG. **10**) with limited attenuation. However, light propagating in a direction parallel to the interface between the bonded die and the silicon layer (i.e., into the plane of the image) will experience greater propagation losses. As will be evident to one of skill in the art, the waveguide **1030** will support a fundamental mode with a substantially Gaussian mode profile. Thus, embodiments of the present invention utilize metal-assisted bonds outside the waveguide and partial metal-assisted bonds in the waveguide region. The partial metal-assisted bond includes a first portion with little attenuation (and greater transparency) due to the direct bond adjacent the center of the fundamental mode and a second portion with acceptable attenuation in the wings of the mode underlying the patterned metal layer **1044**. As discussed above, the optical loss in the direct bond regions is less than in the metal-assisted bonded regions. Thus, system designers can utilize the patterning of the metal layer to provide sufficient bond strength in the metal-assisted bonding areas and low optical loss in the direct bond regions as appropriate to the particular application.

In some embodiments, evanescent coupling can also be used with higher order modes, including more than one maximum in the electric field and intensity profile of the higher order mode. In these embodiments, a node in the electric field of the higher order mode would be aligned with the bond interface, which is characterized by higher loss that other portions of the waveguide. Operation of the higher order mode with such a field distribution would reduce propagation losses because the field intensity would be lower in the high-loss region. One of ordinary skill in the art would recognize many variations, modifications, and alternatives.

Utilizing the combination of direct semiconductor/semiconductor bonds and metal-assisted semiconductor/semiconductor bonds, a hybrid bonding approach is provided that features the benefits of both types of bonds, thereby reducing or overcoming the disadvantages of low temperature semiconductor/semiconductor bonding including the weak interface. Thus, embodiments of the present invention provide for high strength bonds (metal-assisted bond **1042**) while enabling low optical loss in regions of the structure suitable for light propagation (direct bond **1040**).

Referring to FIG. **10**, in application in which evanescent coupling is used to guide light from the waveguide section to the bonded die, patterning of the metal used for metal-assisted bonding of the die is used to minimize optical loss at the points of greatest field intensity in waveguide **1030**.

FIG. **11** is a simplified side view illustrating a composite-bonded die joined to a silicon photonic substrate including direct coupling according to an embodiment of the present invention. In the waveguide received illustrated in FIG. **11**, edge coupling is used to directly couple light into the absorption region of the bonded die. As illustrated in FIG. **11**, the bonded die is recessed into the silicon layer **712** so that the waveguide in the silicon photonic structure (not illustrated) is coupled into a corresponding waveguide present in the bonded die. As discussed in relation to FIG. **10**, patterning of a metal layer or a metal alloy layer can be performed to provide both bond strength and low optical loss in a predetermined spatial manner.

As illustrated in FIG. **11**, variations on evanescent coupling techniques are provided by embodiments of the present invention. A variety of devices, for example, a composite APD, could be fabricated using this approach, with absorption taking place in the bonded die and multiplication taking place in the silicon below.

Embodiments of the present invention are useful in the fabrication of an APD or a PIN photodiode. In implementations using either evanescent coupling or direct coupling, the photodiode structure may fully reside in the bonded die, or the bonded die may form the absorption region of a hybrid photodiode with, for example, the avalanche structure residing in the silicon layer **1012**. In embodiments utilizing edge coupling, the photodiode may be implemented as a stripe as well as other suitable geometries, including round mesa devices. One of ordinary skill in the art would recognize many variations, modifications, and alternatives.

FIG. **12** is a simplified flowchart illustrating a method of fabricating a composite integrated optical device according to an embodiment of the present invention. The method **1200** includes providing a substrate including a silicon layer (**1210**) and forming a waveguide in the silicon layer (**1212**). As an example, the substrate can be a silicon on insulator (SOI) wafer including a silicon substrate, an oxide layer disposed on the silicon substrate, with the silicon layer disposed on the oxide layer.

The method also includes forming a layer comprising a metal material coupled to the silicon layer (**1214**) and providing an optical detector (**1216**). A variety of optical detectors are included within the scope of the present invention, including an APD receiver, a PIN receiver, or the like. Forming the layer comprising the metal material can include depositing the metal material and patterning the metal material to expose the silicon layer in a predetermined spatial pattern. The metal material can include In_xPd_y (e.g., $In_{0.7}Pd_{0.3}$) or other suitable metals and/or metal alloys. The thickness of the metal material can be extremely thin, for example, less than 100 Å in thickness.

The method further includes forming a metal-assisted bond between the metal material and a first portion of the optical detector (**1218**) and forming a direct semiconductor-semiconductor bond between the waveguide and a second portion of the optical detector (**1220**). Low temperature bonding processes are included within the scope of the present invention and forming the metal-assisted bond and forming the direct semiconductor-semiconductor bond can include performing one or more bonding processes at a temperature ranging from about 350° C. to about 500° C., for example, between about 400° C. and about 450° C.

It should be appreciated that the specific steps illustrated in FIG. **12** provide a particular method of fabricating a composite integrated optical device according to another embodiment of the present invention. Other sequences of steps may also be performed according to alternative embodiments. For example, alternative embodiments of the present invention may perform the steps outlined above in a different order. Moreover, the individual steps illustrated in FIG. **12** may include multiple sub-steps that may be performed in various sequences as appropriate to the individual step. Furthermore, additional steps may be added or removed depending on the particular applications. One of ordinary skill in the art would recognize many variations, modifications, and alternatives.

It is also understood that the examples and embodiments described herein are for illustrative purposes only and that various modifications or changes in light thereof will be suggested to persons skilled in the art and are to be included within the spirit and purview of this application and scope of the appended claims.

What is claimed is:

1. A composite integrated optical device comprising:
- a complementary metal oxide semiconductor (CMOS) substrate comprising a silicon layer;
- a waveguide disposed in the silicon layer;
- an optical detector bonded to the silicon layer comprising; and
- a bonding region disposed between the silicon layer and the optical detector, wherein the bonding region comprises:
  - a metal-assisted bond at a first portion of the bonding region, wherein the metal-assisted bond includes an interface layer positioned between the silicon layer and the optical detector; and
  - a direct semiconductor-semiconductor bond at a second portion of the bonding region.

2. The composite integrated optical device of claim **1** wherein the metal-assisted bond provides an ohmic contact between the optical detector and the silicon layer.

3. The composite integrated optical device of claim **1** wherein the metal-assisted bond provides a Schottky contact between the optical detector and the silicon layer.

4. The composite integrated optical device of claim **1** wherein the CMOS substrate comprises a silicon on insulator wafer.

5. The composite integrated optical device of claim **1** wherein the optical detector comprises a III-V optical device.

6. The composite integrated optical device of claim **1** wherein the III-V optical device comprises an APD receiver.

7. The composite integrated optical device of claim **1** wherein the interface layer comprises In_xPd_y.

8. The composite integrated optical device of claim **7** wherein x=0.7 and y=0.3.

9. The composite integrated optical device of claim **1** wherein a thickness of the interface layer is less than 100 Å.

10. The composite integrated optical device of claim **9** wherein the thickness is less than 50 Å.

11. The composite integrated optical device of claim **1** wherein the waveguide supports a fundamental mode and a first portion of the waveguide associated with a maximum intensity of the fundamental mode includes a direct semiconductor-semiconductor bond and a second portion of the waveguide associated with a wing of the fundamental mode includes a metal-assisted bond.

12. The composite integrated optical device of claim **1** wherein the waveguide supports a higher order mode and a node of the higher order mode is positioned at a metal-assisted bond.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 8,611,388 B2
APPLICATION NO. : 13/040184
DATED : December 17, 2013
INVENTOR(S) : Stephen B. Krasulick et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims:

In Column 12, line 21, Claim 1: please delete "comprising"

Signed and Sealed this
Thirtieth Day of August, 2016

Michelle K. Lee

Michelle K. Lee
Director of the United States Patent and Trademark Office